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1. (Amended) A method of implementing a digital communications link connecting a digital controller section of an xDSL modem, located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be substantially free of electronic noise from other electronic components on the motherboard which could significantly affect the overall operation of such xDSL modem, said method comprising the steps of:

   (a) providing a plurality of receive signal lines for communicating data from a remote xDSL modem;

   (b) providing a plurality of transmit signal lines for communicating data to a remote xDSL modem;

   (c) providing a bit clock signal line separate from said plurality of receive signal lines and said plurality of transmit signal lines for carrying a bit clock signal, which bit clock signal is generated by scaling a separate clock signal useable by the xDSL modem, such that said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

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2. (Amended) The method of claim 1, further including a step: providing a reset signal to reset the analog section of the xDSL modem.

3. (Original) The method of claim 1, wherein at least four (4) signal lines are used for said receive signal lines, and at least (4) separate signal lines are used for said transmit signal lines.

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4. (Amended) The method of claim 1, further including a step of providing a word clock signal, which word clock signal has a cycle consisting of at least four (4) bit clock cycles, with the first cycle being a first value and the remaining cycles being a second value.

5. (Original) The method of claim 1, wherein said receive and/or transmit signal lines can also be used for implementing an embedded operation channel within said receive and/or transmit signal lines, said embedded operation channel consisting of control signals embedded in both transmit and receive directions for use by the xDSL modem.

6. (Original) The method of claim 4, wherein at least one (1) bit per word clock cycle is used to carry control signals.

7. (Amended) The method of claim 5, wherein each control signal can have a first or a second length.

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8. (Original) The method of claim 5, wherein each control signal begins with a start bit, is followed by a length bit, then by a set of command bits, and then idle bits are sent between control signals.

9. (Amended) The method of claim 1, further including a step: providing a multi-channel data frame during a plurality of consecutive bit clock periods based on said bit clock signal, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame, and further wherein said first and second time periods occur within said plurality of consecutive bit clock periods.

10. (Amended) The method of claim 9, wherein the number of channels in the multi-channel data frame is programmable.

11. (Amended) The method of claim 9, wherein said plurality of consecutive bit clock periods consists of at least four (4) bit clock cycles for each channel.

12. (Amended) The method of claim 11, wherein the boundary of each multi-channel data frame is indicated by a separate word clock signal having a first predetermined value at the frame beginning and a second predetermined value in the rest of the frame.

13. (Original) The method of claim 1, wherein said same receive and/or transmit signal lines can also be used to support a data interface between said digital controller and a hardware or DSP based xDSL modem.

14. (Original) The method of claim 13, wherein the data interface is logically equivalent to a Utopia I and/or II interface and said hardware or DSP based xDSL modem also can perform an ATM transport convergence (TC) function.

15. (Original) The method of 14, wherein an embedded operation channel (EOC) is used to control proper operations of the hardware or DSP based xDSL modem.

16. (Amended) The method of claim 1, wherein said separate clock signal is based on a master clock external to the xDSL modem and operated at a frequency required by the digital communications link.

32. (Amended) A method of implementing a digital communications link within a personal computer system, comprising the steps of:

(a) providing a plurality of receive signal lines, said receive signal lines being configurable such that data can be received by a digital controller from both an analog codec and an ATM interface;

(b) providing a plurality of transmit signal lines, said transmit signal lines being configurable such that data can be transmitted by a digital controller to both an analog codec and an ATM interface;

(c) providing a clock signal line, said clock signal line carrying a clock signal adapted for data transfers associated with both an analog codec and an ATM interface;

(d) providing a data transfer protocol such that data transfers over said digital communications link can include codec samples and/or ATM cell data;

wherein said bit clock further can be varied to accommodate a plurality of different data transfer protocols used in the digital communications link.

33. (Original) The method of claim 32, wherein said ATM interface is logically equivalent to an ATM Utopia I and II interfaces.

34. (Amended) The method of claim 32, wherein the digital controller is located on a system motherboard of the personal computer system, and said analog codec is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog codec.

35. (Amended) The method of claim 32, wherein said digital communications link supports a plurality of data channels by time division multiplexing data transfers using a frame signal related to said clock signal.

36. (Amended) The method of claim 32, wherein operational and/or control information for said analog codec and/or can be embedded in data frames communicated through the plurality of receive and transmit signal lines.

61. (Amended) In a motherboard for use in a personal computing system, and which system is configured to treat a high speed xDSL capable modem as a motherboard device, the improvement comprising:

(A) a digital controller associated with the high speed modem, said digital controller being located physically on the motherboard and including:

[i] circuitry for processing xDSL formatted data and control signals; and

(B) an analog front end circuit associated with the high speed modem, said analog front end circuit being electrically coupled but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to said xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit, said digital interface including:

[i] a plurality of xDSL data receiving lines; and

[ii]a plurality of xDSL data transmitting lines; and

[iii] a clock signal adapted for an xDSL compatible link, said clock signal being generated by scaling a separate clock signal useable by the xDSL capable modem, such that said clock signal is variable to accommodate a plurality of different xDSL transmission protocols; and

wherein said digital interface supports an xDSL compatible data link between said digital controller and said analog front end circuit.

62. (Original) The motherboard of claim 61, wherein said analog front end circuit is located on a riser card which is configured to be mounted substantially perpendicular to the motherboard.

63. (Original) The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

64. (Original) The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

65. (Amended) The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be used to support an Asynchronous Transfer Mode (ATM) interface.

66. (Amended) The motherboard of claim 65, wherein said ATM interface is a Utopia I and/or II interface.

Please add new claims 67 – 120:

67. (New) A method of transmitting data over an xDSL digital communications link between a digital controller portion of an xDSL modem and an analog codec portion of the xDSL modem, comprising the steps of:

(a) selecting an xDSL transmission protocol to be used in the xDSL digital communications link; and

(b) configuring a bit clock to accommodate transmission requirements of said selected xDSL transmission protocol, said bit clock being generated by scaling a separate clock signal useable by the xDSL modem; and

(c) communicating data between the digital controller portion of the xDSL modem and the analog codec portion of the xDSL modem across the xDSL digital communications link using said bit clock; and

wherein said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

68. (New) The method of claim 67, wherein said separate clock signal is a master clock signal used by the xDSL modem, and said bit clock is derived by dividing said master clock signal by a value specified for said xDSL transmission protocol.

69. (New) The method of claim 68, wherein said value specified for said xDSL transmission protocol is programmed and stored in a register of the analog codec portion of the xDSL modem.

70. (New) The method of claim 67, wherein the xDSL digital communications link is embodied as a bus located on a motherboard of a personal computer system.

71. (New) The method of claim 67, wherein said bit clock is used for both receive and transmit data.

72. (New) The method of claim 67, further including a step: (d) generating a word clock based on said bit clock for communicating data words between the digital controller portion of the xDSL modem and the analog codec portion of the xDSL modem across the xDSL digital communications link, said word clock having a period equal to a plurality of bit clock periods.

73. (New) The method of claim 67, further including a step: (d): transmitting a frame of data across the xDSL digital communications link, said frame of data occupying a plurality of consecutive bit clocks.

74. (New) The method of claim 73, wherein said frame of data is transmitted by dividing it over multiple communications lines.

75. (New) The method of claim 73, wherein said frame of data is signalled by a word clock being held in an active state for more than one bit clock period.

76. (New) The method of claim 67, wherein said xDSL transmission protocols include Asymmetric Digital Subscriber Loop (ADSL) protocols.

77. (New) The method of claim 67, wherein said data includes digital samples generated by an analog to digital converted forming part of the analog codec portion of the xDSL modem, and said digital samples are processed by host signal processing circuitry to support the xDSL modem.

78. (New) The method of claim 67, wherein said host signal processing circuitry includes a FFT circuit embedded in a digital controller as well as software executing on a host processor.

79. (New) The method of claim 67, wherein said data includes Asynchronous Transfer Mode (ATM) based data cells, and said ATM based data cells are processed by a hardware based signal processor to support the xDSL modem.

80. (New) The method of claim 67, wherein steps (a), (b) and (c) are performed by the digital controller portion of the xDSL modem incorporated as part of a North Bridge and/or a South Bridge chipset.

81. (New) The method of claim 67, wherein step (c) is performed by the analog codec portion of the xDSL modem which is located on a separate board from the digital controller.

82. (New) The method of claim 67, wherein said bit clock can have a frequency exceeding 35 Mhz.

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83. (New) A system for implementing a digital communications link connecting a digital controller section of an xDSL modem located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be substantially free of electronic noise from other electronic components on the motherboard which could significantly affect the overall operation of such xDSL modem, the system comprising:

(a) plurality of receive signal lines implemented as part of a communications bus within the computing system for communicating data from a remote xDSL modem;

(b) a plurality of transmit signal lines implemented as part of said communications bus for communicating data to a remote xDSL modem;

(c) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal to clock transfers for said communications bus;

wherein said bit clock signal has a variable frequency that can be set to accommodate a plurality of different xDSL transmission protocols.

84. (New) The system of claim 83, wherein said bit clock can have a frequency exceeding 35 Mhz.

85. (New) The system of claim 83, wherein said bit clock signal is generated by the digital controller section integrated in a North Bridge or South Bridge chipset.

86. (New) The method of claim 83, wherein said bit clock signal is generated by the separate analog section of the xDSL modem on a modem riser card.

87. (New) The system of claim 83, wherein the system is incorporated within a North Bridge and/or a South Bridge chipset.

88. (New) The system of claim 83, wherein the system is incorporated within a motherboard for a computer system.

89. (New) The system of claim 83, further including an interface for transferring data over a USB based bus.

90. (New) The system of claim 89, further including an interface for transferring data over an AC – 97 based bus.

91. (New) The system of claim 90, further including an interface for transferring data over a PCI bus.

92. (New) A communications protocol for transmitting data over a digital communications link within a computer system between a digital controller and an analog coder/decoder (CODEC), the protocol comprising the steps of:

(a) generating a bit clock adapted for data transmission requirements of the digital communications link;

(b) generating a separate frame signal for indicating a boundary for a variable sized data frame transmitting the data between the digital controller and the analog CODEC;

(c) supporting a scaleable data rate in the digital communications link by adjusting a clock rate of said bit clock and/or a size of said variable sized data frame.

93. (New) The communications protocol of claim 92 wherein said clock rate is varied in accordance with an xDSL transmission standard used in the digital communications link.

94. (New) The communications protocol of claim 92 wherein said size of said variable sized data frame is adjusted by changing a number of active data channels used in the digital communications link.

95. (New) The communications protocol of claim 94 wherein said number of active data channels can be varied in both a transmit and receive direction in the digital communications link.

96. (New) The communications protocol of claim 94 wherein said number of active data channels is programmed by the digital controller.

97. (New) The communications protocol of claim 94 wherein said number of active data channels is used to support a plurality of separate communication links with a plurality of respective separate analog codecs.

98. (New) The communications protocol of claim 92 wherein said frame signal is based on a word clock signal, said word clock signal being used for clocking a sample data word from an analog to digital (A/D) converter in the CODEC.

99. (New) An input/output (I/O) circuit for supporting a communications link over a computer bus used within a computer system between a digital controller and an analog coder/decoder (CODEC), the I/O circuit including:

a digital communications interface including:

1) a plurality of receive lines for receiving data; and

2) a plurality of transmit lines, separate from said plurality of receiving lines, for transmitting data;

wherein the data is transferred in parallel across said plurality of receive lines and said plurality of transmit lines in accordance with the bus protocol;

3) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal adapted for a transmission protocol supported by the bus protocol;

4) a frame clock signal line for carrying a frame clock signal adapted for clocking a variable sized data frame in accordance with the bus protocol, said variable sized data frame having a size based on a number of active channels in the plurality of separate data channels and/or a desired data rate;

wherein said plurality of receive lines, said plurality of transmit lines, said bit clock signal line and said frame clock signal line support the bus protocol as part of the communications bus within the personal computer system.

100. (New) The I/O circuit of claim 99 wherein said clock rate is varied in accordance with an xDSL transmission standard used in the digital communications link.

101. (New) The I/O circuit of claim 99 wherein said size of said variable sized data frame is adjusted by changing a number of active data channels used in the digital communications link.

102. (New) The I/O circuit of claim 101 wherein said number of active data channels can be varied in both a transmit and receive direction in the digital communications link.

103. (New) The I/O circuit of claim 101 wherein said number of active data channels is programmed by the digital controller.

104. (New) The I/O circuit of claim 101 wherein said number of active data channels is used to support a plurality of separate communication links with a plurality of respective separate analog CODECs.

105. (New) The I/O circuit of claim 99 wherein said frame signal is based on a word clock signal generated by the digital interface, said word clock signal being used for clocking a sample data word from an analog to digital (A/D) converter in the CODEC.

106. (New) A method of communicating data between a first integrated circuit located on a computer motherboard and a second integrated circuit located on the computer motherboard, the method comprising the steps of:

(a) communicating transmit data from the first integrated circuit to the second integrated circuit using a plurality of data transmit signal lines for; and

(b) communicating receive data from the second integrated circuit to the first integrated circuit using a plurality of data receive signal lines, wherein said data receive signal lines are separate from said data transmit signal lines; and

wherein both transmit and receive data can be communicated at the same time between said first integrated circuit and said second integrated circuit over said plurality of data transmit signal lines and said plurality of data receive signal lines;

(c) providing a first clock signal on a first clock signal line, said first clock signal being adjustable based on a transmit transfer rate to be used for said transmit data; and

(d) providing a second clock signal on a second clock signal line, said second clock signal being adjustable based on a receive transfer rate to be used for said receive data;

wherein both said transmit transfer rate and said receive transfer rate can be independently configured for data communications between the first integrated circuit and the second integrated circuit.

107. (New) The method of claim 106 wherein a transmit data word is clocked in parallel over said plurality of data transmit signal lines, such that a first portion of said data word is transferred over a first data transmit signal line of said plurality of data transmit signal lines, and a successive second portion of said data word is transferred over a separate second data transmit signal line of said plurality of data transmit signal lines.

108. (New) The method of claim 106 where said first portion is a bit, and said first clock signal is a bit clock.

109. (New) The method of claim 106 wherein both a scaleable transmit transfer rate and a scaleable receive transfer rate can be generated based on a value set in a control register within the second integrated circuit.

110. (New) The method of claim 106 wherein the first integrated circuit and second integrated circuit are coupled by an asymmetric communications link in which said transmit transfer rate and said receive transfer rate differ substantially from each other.

111. (New) The method of claim 106 wherein said transmit transfer rate and/or said receive transfer rate are also configurable by adjusting a number of time slots used within a transmit frame and/or a receive frame communicated between the first integrated circuit and the second integrated circuit.

112. (New) The method of claim 111 wherein said transmit frame and/or said receive frame can be configured to set up multiple communications channels between the first integrated circuit and a plurality of second integrated circuits.

113. (New) A method of communicating data over a data link connecting a first integrated circuit located on a computer motherboard and a second integrated circuit located on the computer motherboard, the method comprising the steps of:

(a) communicating first transmit data from the first integrated circuit to the second integrated circuit over the data link using a first transmission channel; and

(b) communicating first receive data from the second integrated circuit to the first integrated circuit over the data link using a first receive channel, said first receive channel and said first transmission channel being separate; and

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a scaleable clock signal;

wherein said scaleable clock signal is adjusted for the data link between the first integrated circuit and the second integrated circuit so that the data link uses a scaleable clock rate to support a data transfer rate required for said first transmission channel and/or said first receive channel.

114. (New) The method of claim 113 further including a step of setting up a second transmission channel and a second receive channel over the data link between the first integrated circuit and a third integrated circuit to support second transmit data and second receive data respectively using said scaleable clock signal.

115. (New) The method of claim 113 wherein said scaleable clock rate is used to generate a transmit clock rate used in said first transmission channel and a separate receive clock rate used in said first receive channel, such that said transmit clock rate and said separate receive clock rate are related by an integer ratio.

116. (New) The method of claim 115 wherein said integer ratio is provided in a control register in the second integrated circuit

117. (New) The method of claim 113 wherein said scaleable clock signal is a bit clock used in both said first transmit channel and said first receive channel.

118. (New) The method of claim 113 wherein said data link is set up over a computer bus located on the computer motherboard.

119. (New) The method of claim 113 further including a step of providing a data word clock for effectuating said data transmissions in the form of data words transferred over the data link, said data words including a fixed number of data bits such that said data word clock has a period corresponding to multiple scaleable clock signals.

120. (New) The method of claim 113 further including a step: time division multiplexing control information and data over said first transmission channel so as to provide control information from the first integrated circuit to said second integrated circuit as part of said data transmission, said control information including a power management signal including at least a wake-up signal and/or a power down signal.